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Semiconductor processing apparatus, method of making and use of same.

Abstract:

Abstract of EP0635869

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(54) Semiconductor processing apparatus, method of making and use of same.

(57) A wafer support apparatus used for electrostatic clamping of a wafer to the wafer support is disclosed, wherein a dielectric material, formed on the surface of a wafer support facing the wafer to facilitate the electrostatic clamping, has a protective coating formed over the dielectric material to provide protection to the dielectric material against chemical attack from chemicals used during the processing of the semiconductor wafer. In a preferred embodiment, the protective coating comprises an aluminum compound, such as an oxide of aluminum or aluminum nitride, having a thickness ranging from 1 μm to 30 μm, but not exceeding about 50% of the thickness of the dielectric material so as to not interfere with the electrostatic charge used for clamping the wafer to the wafer support. Also disclosed is a method for making the wafer support apparatus to protect the dielectric material on a wafer support, and use of same in a process for forming integrated circuit structures.

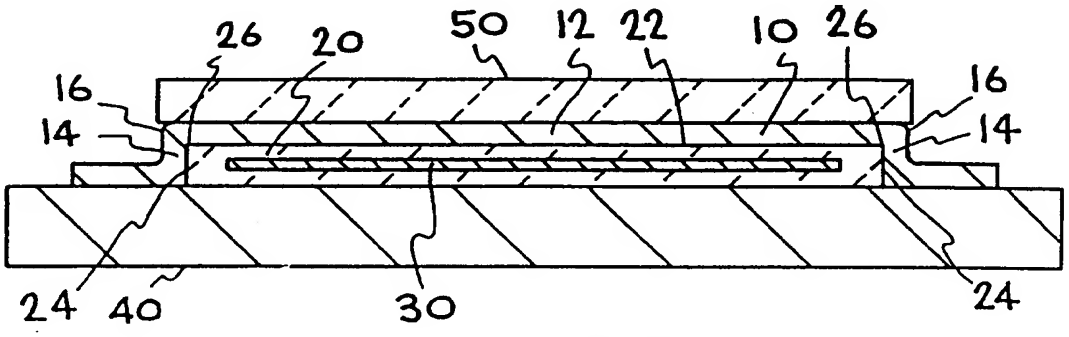

FIG. 1

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This invention relates to a semiconductor processing apparatus, a method of making and use of same.

In the processing of semiconductor wafers in a sealed chamber to form integrated circuit structures thereon, the semiconductor wafer is normally positioned on a wafer support within the chamber. To secure the wafer to the support, and in particular to prevent movement of the wafer (either vertically or laterally) during processing, it has been customary to physically clamp the wafer to the underlying support.

More recently however, other means for securing the wafer to the support have been explored and adopted due to various problems, such as particle formation, mechanical stress, etch profiles, etc., which have been experienced with the use of mechanical force to secure the wafer to the support.

One such wafer securement means, commonly referred to as electrostatic clamping, utilizes an electrostatic charge on the surface of a dielectric material formed over the portion of the metal wafer support facing the wafer, i.e., between the undersurface of the wafer and the facing surface of the underlying metal wafer support. Such electrostatic clamping is described, for example, in Abe U.S. Patent 4,384,918; Japan Patent Document 2-27748; and in "Electrostatic Force and Absorption Current of Alumina Electrostatic Chuck", published by Watanabe et al. in Jpn. Journal of Applied Physics, Vol. 31(1992) at pages 2145-2150.

While this type of wafer securement, utilizing electrostatic clamping, has proved to be successful in eliminating the previous problems encountered in the mechanical clamping of the wafer to the wafer support, corrosion problems have been encountered because the dielectric materials which provide the most satisfactory performance in the use of electrostatic clamping to secure the wafer to the wafer support do not exhibit sufficient resistance to some of the chemicals used during the processing of the semiconductor wafer in the chamber.

In particular, when a polyimide material is provided, as the dielectric material, on the top surface of the metal wafer support, it has been found that such polyimide material is susceptible to chemical attack by O_2 gas, used for in situ cleaning of the chamber after etching. The polyimide material has also been found to be subject to chemical attack by fluorine-containing gases as well, although to a lesser extent thin the vulnerability to O_2, attack.

It therefore would be desirable to provide protection against chemical attack for the dielectric material; formed on the surface of the metal wafer support for the purpose of electrostatic clamping of a semiconductor wafer to the wafer support, without however, interfering with the electrostatic charge on the surface of the dielectric material.

This object is solved by the semiconductor processing apparatus according to independent claims 1 or 5, the process for providing protection to a dielectric material according to independent claim 15 and the process for forming integrated circuit structures according to independent claim 18. Further advantageous features, aspects and details of the invention are evident from the dependent claims, the description and the drawings. The claims are intended to be understood as a first non-limiting approach of defining the invention in general terms.

The invention provides a protective coating for dielectric material on wafer support used in integrated circuit processing apparatus and method of forming same.

According to a specific aspect of the invention a protective coating is formed over a dielectric layer, used for electrostatically clamping a semiconductor wafer to a wafer support in integrated circuit processing apparatus, to protect the dielectric layer from chemical attack; further a method of protecting the dielectric layer is provided.

The invention according to a preferred aspect provides an improvement in the field of electrostatically clamping a semiconductor wafer to a wafer support having a dielectric material formed on the surface thereof facing the wafer. The improvement is achieved by a protective coating formed over the dielectric surface to provide protection to the dielectric material against chemical attack from chemicals used during the processing of the semiconductor wafer; according to a further aspect a method for protecting the dielectric material is provided by forming the protective layer over the dielectric material in a manner which will not interfere with the formation of a sufficient electrostatic charge on the coated wafer support surface facing the wafer to secure the wafer to the wafer support without either vertical or lateral movement of the wafer during processing.

Figure 1 is a vertical cross-sectional view of a wafer support according to an embodiment of the invention showing a dielectric layer formed on the wafer support surface thereon, and a protective layer formed over the exposed surfaces of the dielectric material.

Figure 2 is a pictorial side view of an apparatus which may be used in forming the protective coating over the dielectric material on the wafer support.

The invention provides a protective coating formed over a dielectric material provided on a wafer support in a semiconductor wafer processing apparatus to electrostatically clamp the wafer to the support; and it also provides a method of forming

the protective coating over the dielectric material without interfering with the desired electrostatic clamping of the wafer to the wafer support.

The dielectric material to be protected may comprise any non-conductive material formed over a conductive surface in order to store the desired electrostatic charge thereon. The invention, however, is particularly directed to polymeric dielectric materials such as, for example, polyimide, since such materials, while forming good dielectric materials, are subject to attack by the processing used in the formation of integrated circuit structures on the wafer.

The protective coating formed over the dielectric material basically must comprise a material capable of providing the desired protection of the dielectric material especially against chemical attack by chemicals used to process the semiconductor wafer, without interfering with the desired electrostatic clamping provided by the dielectric material. The protective material must also be compatible with the various processes carried out in the apparatus containing the wafer support during the course of forming integrated circuit structures on the semiconductor wafer, e.g., not react with, nor interfere with the chemicals used in the processing of the semiconductor wafer.

The protective coating formed over the dielectric material should advantageously be rather thin so as to not interfere with the establishment of the desired electrostatic charge on the dielectric surface facing the wafer. It has been found that the strength of this electrostatic chucking force is inversely proportional to the square of the thickness of the dielectric material. In general it has been found that the thickness of the protective coating should not exceed about 50% of the thickness of the dielectric material to be protected, and preferably not exceed about 10% of the dielectric material, to ensure that the protective coating is not so thick that it interferes with the electrostatic charge formed on the surface over the dielectric layer. Usually the protective coating need not exceed about 30 microns to provide the desired chemical protection, and preferably the protective coating will not exceed about 10 microns in thickness.

The protective coating should preferably be uniform in thickness, both for the desired chemical protection and for uniformity of the electrostatic charge strength through the coating from the underlying dielectric material. Furthermore, the coating should be conformal, with respect to uniformity of coating thickness, not only over the flat surface portions of the wafer support and dielectric surface thereon, but also at comers as well. By uniform in thickness is meant that the thickness of a given protective coating does not vary by more than about ±5% from the mean thickness, using a typical 9 point measurement pattern. It should be noted that if necessary, the sharpness of the comers of the underlying dielectric material may be rounded or slanted, if-desired, to achieve the desired uniformity of the thickness of the protective coating layer.

As stated above, the protective coating should be capable of withstanding chemical attack by processing materials such as etch mateals used in processing the semiconductor wafer. In particular, the protective coating should be capable of providing protection to the underlying dielectric material from attack by etchants such as O_2-containing etchants or fluorine-containing etchants. Generally a minimum thickness of the protective coating of at least about 1 micron, and preferably about 3 microns, will ensure a sufficient thickness to provide the desired degree of protection for the underlying dielectric material. However, not only is a minimum and uniform thickness of protective coating required , but there also must be an absence of any pinholes or openings in the protective coating. By an absence of any pinholes is meant that no pinholes are visible to inspection of the protective coating by scanning electron microscopy (SEM).

As a further property of the protective coating, the thermal coefficient of expansion of the protective coating should advantageously sufficiently match, or be compatible with both the dielectric material and the metal support on which the dielectric material is formed, up to a temperature of about 150 °C, so as to avoid cracking or the inducement of mechanical stresses in the underlying dielectric material. By "sufficiently match" is meant that the thermal coefficient of expansion of the protective coating does not vary from either the thermal coefficient of expansion of said wafer support or the thermal coefficient of expansion of the dielectric material by more than about 20%.

The protective coating should also be physically strong enough to resist particle penetration by any particles which may be normally encountered in normal semiconductor wafer processing. That is, the protective coating should be capable of providing mechanical protection to the dielectric material which may be soft and therefore susceptible to particle penetration. While the formation of the dielectric material on the wafer support, and the formation of a electrostatic charge on the wafer support thereby, form no part of the instant invention, one manner in which the desired electrostatic charge is formed on the surface of the dielectric material is by the provision of a metal electrode embedded in the dielectric material. If a particle should penetrate into the dielectric material sufficiently to contact such a buried electrode, such formation of the desired electrostatic charge could be impeded. The protective layer thus should be

capable of affording mechanical protection against such penetration, as well as providing the desired chemical protection.

Finally, the protective coating should be sufficiently conductive to permit release of the electrostatic charge when the wafer is to be removed from the wafer support, yet sufficiently insulative to hold the electrostatic charge on the surface during the clamping or chucking of the wafer to the wafer support. Usually a protective material having a resistivity ranging from about 10^{13} ohm centimeters (Ω cm.) to about 10^{20} Ω cm. will be found to be satisfactory from a standpoint of conductivity versus resistivity.

When the metal wafer support on which the dielectric material is mounted comprises an aluminum material, it has been found that an inorganic aluminum compound, such as a oxide of aluminum (e.g., Al_2O_3) or aluminum nitride (AlN) formed to a thickness ranging from about 1 micron to about 30 microns, and preferably to a thickness of from about 3 microns to about 20 microns, and not exceeding about 50% of the thickness of the dielectric material, will meet all of the above requirements.

The protective coating may be formed over the dielectric material and exposed areas of the wafer support by a deposition process such as an ion-assisted (E-beam) evaporation process, or by a plasma spray process, or by a CVD process. Preferably, during the deposition of the protective coating, the wafer support and dielectric material thereon are located or positioned above the protective material source to prevent or at least inhibit the deposition of any particles on the dielectric material and/or wafer support during deposition of the protective material.

By way of illustration, and not of limitation, when an ion-assisted evaporation process is used to deposit the protective coating over the wafer support and dielectric material thereon, the beam power may be several kW; the wafer support to be coated may be located about 50.8 cm (20 inches) from the coating source being evaporated by the beam; the temperature may range from about room temperature up to about 150 °C; the pressure may be as low as possible, preferably ranging from about 13 to about 133 Pa (about 0.1 to about 1 Torr); and the time may vary from about 1 to about 24 hours, depending on the temperature and beam power level.

Referring now to Figure 1, an example of the protective coating of the invention is shown at 10 covering the exposed surfaces of a dielectric material 20, which may have an electrode 30 therein to assist in the desired generation of an electrostatic charge on the surface of dielectric material 20. Dielectric material 20 is, in turn, secured to a surface of a metallic wafer support 40 which conventionally may comprise aluminum or an aluminum alloy, i.e. , a alloy containing at least about 50 wt. % aluminum. The structure is further shown, for illustrative purposes only, having a wafer 50 thereon, it being understood that the wafer is not present while the protective coating 10 is being formed over dielectric material 20 and metallic wafer support 40. It will be understood that the relative thicknesses of the materials shown in the drawings is not to scale, with the thickness of some of the materials exaggerated for illustrative purposes only.

As previously discussed, protective coating 10 should comprise a material capable of forming a conformal coating over the surfaces of dielectric material 20. In particular, portion 12 of protective coating 10, formed over the flat surface 22 of dielectric layer 20 to which wafer 50 will adhere due to the electrostatic charge thereon, should be approximately the same thickness as portion 14 of protective coating formed on the end edges 24 of dielectric material 20 and the protective coating portion 16 formed over the corners 26 of dielectric material 20. Such a conformal coating of dielectric material 20 by protective coating material 10 will result in a uniformity of the desired chemical protection, as well as permitting a uniform charge distribution of the electrostatic charge across the surfaces contacted by wafer 50.

Now referring to Figure 2, a typical apparatus 100 which can be used for the formation of protective coating 10 on dielectric material 20 and metal wafer support 40 is illustrated. In the illustrated embodiment, apparatus 100 comprises an ion assisted (E-beam) type deposition apparatus having a deposition chamber 110 with a clamping mechanism 120 therein comprising a pedestal 126 with clamping fingers 124 which will engage the peripheral portion of metallic wafer support 40 not covered by dielectric material 20 to urge wafer support 40 against pedestal 126. Preferably, as shown, clamping mechanism 120 will be located or positioned adjacent the top of chamber 110 to avoid any particle deposition onto dielectric material 20, as previously discussed.

Located adjacent the bottom of chamber 110 is a containment vessel, such as illustrated crucible 130, containing the protective material, e.g., Al_2O_3 or AlN, to be coated over the exposed surfaces of dielectric material 20 id metallic wafer support 40. Also shown mounted to the bottom of chamber 110 is a charged particle beam source 140 from which an electron or ion beam 144 may be generated and projected into chamber 110. In the illustrated embodiment, magnetic deflection means 150 within chamber 110 deflect beam 144 toward and into crucible 130 to thereby strike and vaporize the

protective material therein.

By way of illustration, a 196 millimeter (mm) diameter aluminum wafer support, having a 50 micrometer (μm) thick polyimide layer formed thereon, was coated, in accordance with the invention, with a 4 μm thick protective coating of aluminum oxide. The aluminum oxide coating was deposited by evaporating aluminum oxide from a crucible placed 50.8 cm (20 inches) beneath the wafer support and dielectric material thereon in a chamber maintained at a temperature of about 100 °C id at a pressure of about 1 . 3 mPa (about 10^{-5} Torr). The aluminum oxide Was evaporated from the crucible and coated over the dielectric material for a period of about 12 hours, using a ion beam at a power level of about 1.5 kW.

The resulting aluminum oxide protective coating was examined for pinholes under SEM and none were found. To test the coating deposited over the wafer support and dielectric material, the structure was exposed to an O_2 gas plasma for about 8 hours at an average temperature of about 90 °C. The structure was then examined for chemical attack on the underlying polyimide dielectric material. None was found.

The uniformity of the protective coating was also determined by optical nanospec, using a dummy coating (a coating not on an actual polyimide layer), and found to have a thickness variation of less than about 2-3% from the thickest portion to the thinnest portion.

To further test the protective coating, a number of semiconductor wafers were sequentially electrostatically clamped to a semiconductor wafer support mounted in an etch chamber and having a dielectric material affixed to the surface facing the wafer. The wafer support was provided with a protective coating over the dielectric material, in accordance with the invention. After conducting a normal oxide etch on 12 wafers, each of the wafers were examined and found to have not moved during the etch, indicating that the electrostatic clamping had not been adversely affected by formation of the protective coating over the dielectric material. The protective coating on the wafer support was then further examined after such processing for any signs of cracking, indicative of thermal mismatching between the protective coating and the underlying dielectric material and wafer support. None was found. Nor was there any sign of particle impaction damage to the protected dielectric material. Finally, the dielectric material on the wafer support was examined for any indication of chemical attack and none was found.

Thus, the invention provides an improved wafer support utilizing electrostatic clamping wherein the dielectric material, formed on the wafer support in connection with the electrostatic charge utilized in such electrostatic clamping, is protected from chemical attack by chemicals, used in the processing of a semiconductor wafer, in a manner wherein the electrostatic clamping of the wafer is not impaired.

Claims

1. A semiconductor processing apparatus wherein a wafer support has a dielectric material formed thereon to permit clamping of a semiconductor wafer to said wafer support by electrostatic charges, wherein: a protective coating is formed over said dielectric material to protect said dielectric material from attack by chemicals used in processing said semiconductor wafer.

2. The apparatus of claim 1 wherein said wafer support comprises aluminum or an aluminum alloy and/or said protective coating comprises an aluminum compound.

3. The apparatus of any one of the preceding claims wherein said protective coating has a minimum coating thickness of at least 1 μm.

4. The apparatus of any one of the preceding claims wherein said protective coating has a maximum coating thickness not exceeding 30 μm.

5. A semiconductor processing apparatus especially according to any one of the preceding claims wherein a wafer support, comprising aluminum or an aluminum alloy, has a dielectric material formed thereon to permit clamping of a semiconductor wafer to said wafer support by electrostatic charges, wherein: a protective coating comprising an aluminum compound having a minimum thickness of at least 1 μm and a maximum thickness of 30 μm is formed over said dielectric material to protect said dielectric material from attack by chemicals used in processing said semiconductor wafer.

6. The apparatus of any one of the preceding claims wherein said protective coating has a maximum coating thickness which does not exceed about 50% of the thickness of said dielectric material.

7. The apparatus of any one of the preceding claims wherein said protective coating has a maximum coating thickness not exceeding 10 μm.

8. The apparatus of any one of the preceding claims wherein said protective coating is uniform in thickness over said dielectric material to provide uniformity in the strength of said electrostatic charges exerted on said wafer.

9. The apparatus of any one of the preceding claims wherein the thermal coefficient of expansion of said protective coating does not vary from either the thermal coefficient of expansion of said wafer support or the thermal coefficient of expansion of said dielectric material by more than 5 %.

10. The apparatus of any one of the preceding claims wherein said protective coating has a minimum coating thickness of at least about 3 μm.

11. The apparatus of any one of the preceding claims wherein said protective coating is capable of protecting said underlying dielectric material against penetration of said protective coating by particles during processing of said semiconductor wafer.

12. The apparatus of any one of the preceding claims wherein said protective coating has a resistivity ranging from 10^{13} Ω cm to 10^{20} Ω cm to permit holding of said electrostatic charge thereon during said chucking of said wafer and release of said electrostatic charge when said wafer is to be removed from said wafer support.

13. The apparatus of any one of the preceding claims wherein said protective coating comprises an aluminum compound selected from the group consisting of an oxide of aluminum and aluminum nitride.

14. The apparatus of any one of the preceding claims wherein said dielectric material comprises a polyimide material.

15. A process for providing protection to a dielectric material, formed over a wafer support to permit electrostatic clamping of a semiconductor wafer to said wafer support during processing of said wafer, which comprises: forming a protective coating formed over said dielectric material to protect said dielectric material from attack by chemicals used in processing said semiconductor wafer.

16. The process of claim 15 which further comprises forming a protective layer over said dielectric material ranging in thickness from 1 μm to 30 μm, and not exceeding 50% of the thickness of said dielectric material, and comprising an aluminum compound.

17. The process of claims 15 or 16 which further comprises forming a protective layer over said dielectric material comprising an aluminum compound selected from the group consisting of an oxide of aluminum and aluminum nitride.

18. A process for forming integrated circuit structures on a semiconductor wafer wherein said wafer is electrostatically clamped to a wafer support using a dielectric material formed on the surface of said wafer support, wherein: said dielectric material is protected from attack during said formation of said integrated circuit structure on said semiconductor wafer by using a protective coating over said dielectric material capable of withstanding attack by said processing chemicals.

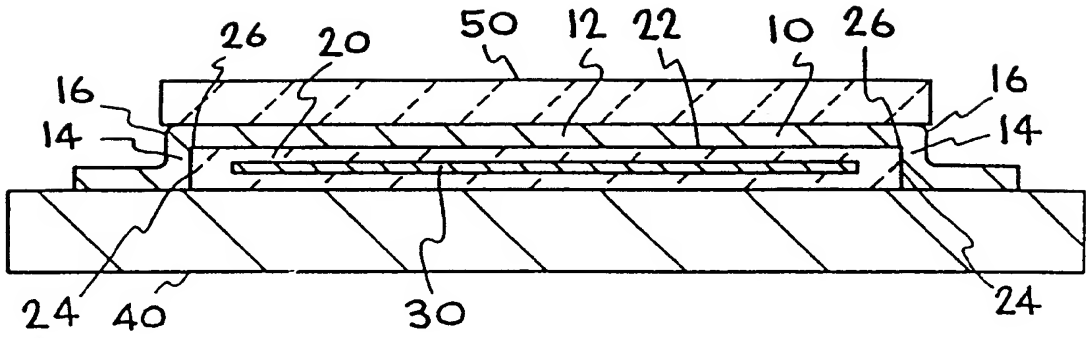
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FIG. 1

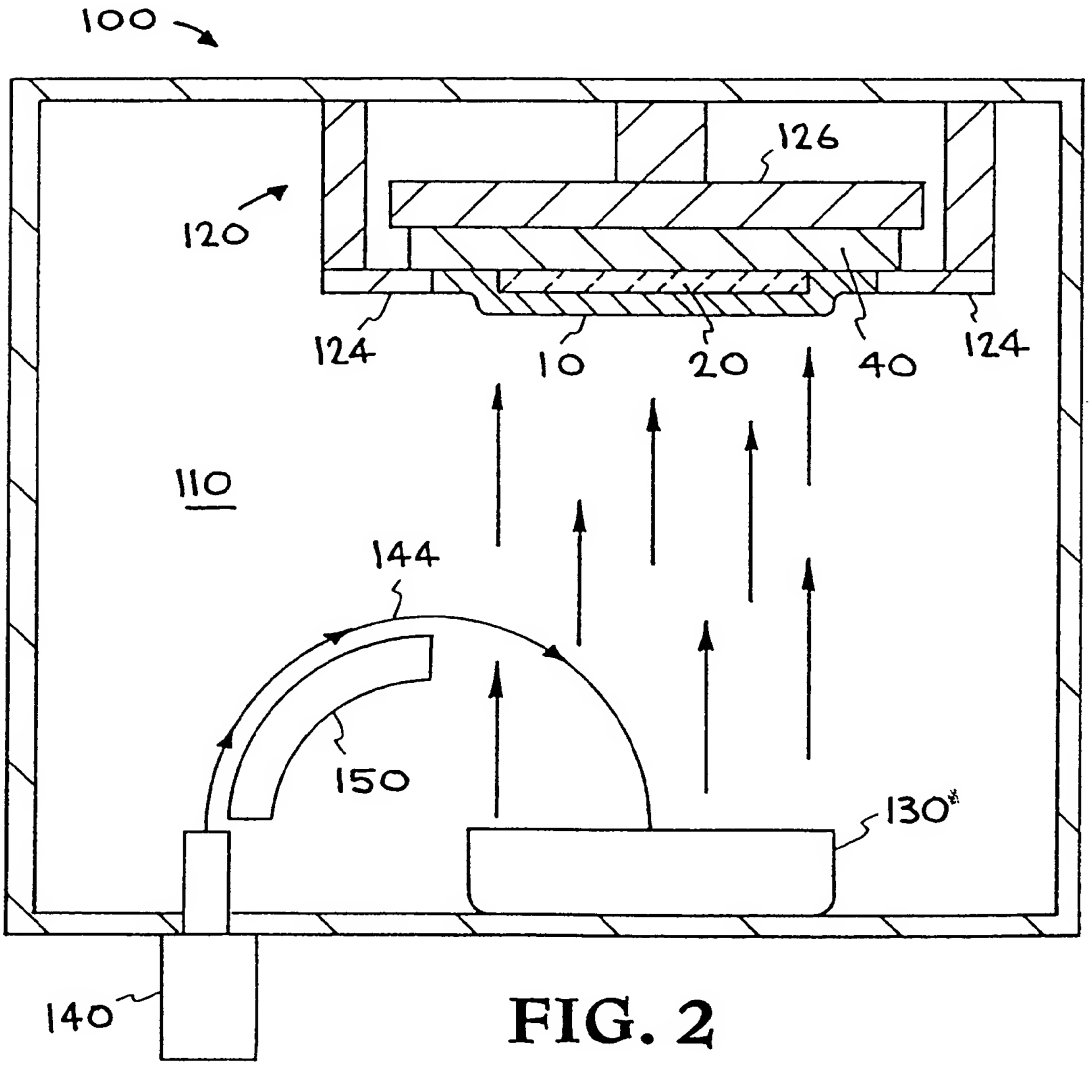
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FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 94 10 6342

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 17, no. 241 (E-1364) 14 May 1993 & JP-A-04 367 247 (KYOCERA CORP) 18 December 1992 * abstract *	1,2,13, 15,17	H01L21/00
X	EP-A-0 452 222 (COMMISSARIAT A L'ENERGIE ATOMIQUE) * column 3, line 15 - column 3, line 34; figure 2 *	1-7,10, 15	
X	EP-A-0 439 000 (APPLIED MATERIALS INC) * page 5, line 32 - page 6, line 36; figure 2 *	1,2,15	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 July 1994	Bolder, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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